OIPE
AUG 1 3 2002
JC130
PATENT & TRADEMARK OFFICE

COPY OF PAPERS ORIGINALLY FILED

#11 Request Recons.

ATTORNEY'S DOCKET ~~NO. A00312770408~~/SJH/MXS

RECEIVED
AUG 22 2002
TECHNOLOGY CENTER 2800

8-28-02
L. Spruell

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Ferguson et al.
Serial No:	09/575,561
Confirmation No:	1264
Filed:	May 21, 2000
For:	METHOD AND APPARATUS FOR USE IN SWITCHED CAPACITOR SYSTEM
Examiner:	Phan, T.
Art Unit:	2818

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

The undersigned hereby certifies that this document is being placed in the United States mail with first-class postage attached, addressed to Commissioner for Patents, Washington, D.C. 20231, on the 5th day of August, 2002.

Steven J. Henry
Reg. No. 27,900

Commissioner for Patents
Washington, D.C. 20231

Sir:

RESPONSE

This responds to the Office Action mailed on February 6, 2002, rejecting all of the claims (claims 1-52). Applicants respectfully submit that all of the pending claims (1-52) are patentable without amendment. Accordingly, Applicants respectfully request reconsideration, removal of the rejection, and allowance of all of the claims.

As an initial matter, Applicants point out that the Office Action does not provide rationale for the rejections of claims 49 (which depends from claim 1) and claim 52 (which is a multiple dependent claim that depends from any of claim 5 or 12). Accordingly, if claims 49 and 52 are not allowed, any subsequent Office Action should be non-final and address each feature of each of those claims.

Rejections of Claims 1-4 and 13-52 Under 35 U.S.C. §103

Paragraph 3 of the Office Action rejects claims 1-4 and 13-52 under 35 U.S.C. 103(a) as being unpatentable over Fling et al., 4,591,832, in view of Mehta et al., 4,205,203, and Lee et al., 6,130,633.

The Office Action first asserts that Fling, as modified by Mehta et al. 4,205,203, teaches all of the features recited in the rejected claims except for "a signal conditioning stage comprising a switched capacitor filter as recited in claims 1-4 and 13-52".

The Office Action further asserts that it would have been obvious to utilize the switched capacitor filter 210 in Fig. 2A of Lee et al. for connecting to the system common output terminal 25 in Fig. 1 of Fling et al. for the purpose of performing lowpass filtering for removal of quantization noise in the system common output analog signal at common output terminal 25 in Fig. 1 of Fling et al.

We shall first address the above-quoted assertion, from paragraph 3 of the Office Action, to the effect that Fling, as modified by Mehta et al., teaches all of the features recited in the rejected claims except for "a signal conditioning stage comprising a switched capacitor filter as recited in claims 1-4 and 13-52". Applicants assume this assertion was not intended to imply that every one of the claims includes "a signal conditioning stage comprising a switched capacitor filter", as such is not true. The phrase "signal conditioning stage" is recited only in claims 1, 5, 29 and 39. The phrase "switched capacitor filter" is recited only in claims 3, 6, 15 and 19 (for example, claim 1 does not refer to a "switched capacitor filter").

Applicants traverse the rejection on two separate grounds, as set forth below.

(I) The proposed motivation is legally insufficient to support the combination. Neither Driscoll, nor Gross, nor any legally sufficient combination thereof, teaches or suggests the inventions recited in claims 2-7, 9-16, 18-32, 34-48, 50-52, 54-55, and 57-61.

The Office Action proposes that one skilled in the art would combine the references as proposed for the purpose of performing lowpass filtering for removal of quantization noise in the system common output analog signal at common output terminal 25 in Fig. 1 of Fling et al.

This proposed motivation is illusory.

First, the Office Action has not presented any evidence in support of the proposed motivation. The proposed motivation is merely a bold, unsupported assertion. The rejection is improper without such evidence. The mere fact that hindsight reveals references could have been combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. (M.P.E.P. §2143.01 citing *In re Mills*). The

teaching or suggestion to make the combination must be found in the prior art, not in Applicant's disclosure (M.P.E.P. §2143 citing In re Vaeck).

Second, observe that Fling itself explicitly teaches away from the proposed combination. Fling et al. discloses a digital-to-analog converter system [that] includes "two DAC's operated in ping pong fashion with their analog output signals linearly summed. To **preclude bandwidth limiting** inherent in the summing operation, the applied digital input signal is preconditioned in accordance with the transfer function $1/(1+Z^{-1})$." (Abstract) (emphasis added). Fling further states that "for most DAC systems, it is desired that the frequency response be at lest as good as the input frequency content. That is, from terminal 10 to terminal 25 **the frequency content should not roll off**." (col. 3, lines 12-15) (emphasis added).

Thus, Fling et al suggests that bandwidth limiting and roll off is to be avoided. Since bandwidth limiting and roll off are natural consequences of lowpass filtering, it is reasonable to assume that lowpass filtering should also be avoided. In view of this teaching in Fling, why would anyone skilled in the art consider adding lowpass filtering to the analog output signals in Fling? He all but expressly says not to! Moreover, as noted in M.P.E.P. §2143.01, the proposed modification cannot render the prior art unsatisfactory for its intended purpose.

Therefore, the proposed combination is improper.

Consequently, neither Fling, nor Mehta, nor Lee, nor any legally tenable combination thereof, teaches or suggests the inventions recited in claims 1-4 and 13-52.

Accordingly, reconsideration and allowance of claims 2-7, 9-16, 18-32, 34-48, 50-52, 54-55, and 57-61 is respectfully requested.

II. Even if Fling, Mehta and Lee were combined as proposed in the Office Action, the proposed combination would not teach or suggest the inventions recited in claims 1-4 and 13-52.

Claims 1, 2-4, 21-28, 49-50 and 52

Claim 1 recites a system comprising "a DAC that receives a multi-bit digital signal and outputs at least two analog signals including a first analog signal and a second analog signal, the first analog signal being indicative of a sum of values of bits in the multi-bit digital signal, the second analog signal also being indicative of **said sum of values of said bits** in the multi-bit

digital signal; and a signal conditioning stage that receives at least two of the at least two analog signals, including the first analog signal and the second analog signal." (emphasis added).

Fling does not teach or suggest a DAC that outputs a "first analog signal being indicative of a sum of values of bits" in a multi-bit digital signal and a "second analog signal also being indicative of **said sum of values of said bits** in the multi-bit digital signal", as recited in claim 1 (emphasis added).

Fling teaches a digital-to-analog converter system that includes two DACs operated in ping-pong fashion with their analog output signals linearly summed (Abstract). In particular, in the system of Fig. 1, digital samples on bus 13 are alternately applied via multiplexor 14 to DACs 16 and 18 (col. 2, lines 37-39). The quantized analog signals are applied to an analog summing circuit 24 which produces the system output signal at terminal 25 (col. 2, lines 52-54).

Thus, Fling teaches that each of the DACs 16 and 18 receives its **own** data bits and outputs one analog signal indicative of a sum of values of those bits. Fling does not show two analog signals being indicative of the same sum of values of bits.

Consequently, the proposed combination does not teach or suggest a system comprising "a DAC that receives a multi-bit digital signal and outputs at least two analog signals including a first analog signal and a second analog signal, the first analog signal being indicative of a sum of values of bits in the multi-bit digital signal, the second analog signal also being indicative of **said sum of values of said bits** in the multi-bit digital signal; and a signal conditioning stage that receives at least two of the at least two analog signals, including the first analog signal and the second analog signal", as recited in claim 1. (emphasis added).

Accordingly, claim 1, and claims 2-4, 21-28, 49-50 and 52 depending therefrom, should now be allowed.

Claims 13-16

Claim 13 recites a method comprising "receiving a multi-bit digital signal; generating at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of **said sum of values of said bits** in the multi-bit digital signal; and filtering at least two of the at least two analog output signals, including the first analog signal and the second analog signal." (emphasis added).

Fling does not teach or suggest generating "a first analog signal that is indicative of a sum of values of bits" in a multi-bit digital signal, and "a second analog signal that is indicative of **said sum of values of said bits** in the multi-bit digital signal", as recited in claim 13 (emphasis added).

As stated above, Fling teaches that each of the DACs 16 and 18 receives its **own** data bits and outputs one analog signal indicative of a sum of values of those bits. Fling does not show two analog signals being indicative of the same sum of values of bits.

Consequently, the proposed combination does not teach or suggest a method comprising "receiving a multi-bit digital signal; generating at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of **said sum of values of said bits** in the multi-bit digital signal; and filtering at least two of the at least two analog output signals, including the first analog_signal and the second analog signal", as recited in claim 13. (emphasis added).

Accordingly, claim 13 and claims 14-16 depending therefrom, should now be allowed.

Claims 17-20

Claim 17 recites a system comprising "means for receiving a multi-bit digital signal; means for generating at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that_is indicative of **said sum of values of said bits** in the multi-bit digital signal; and means for filtering at least two of the at least two analog signals, including the first analog signal and the second analog signal." (emphasis added).

As stated above with respect to claim 13, Fling does not teach or suggest generating a first analog signal that is indicative of a sum of values of bits in a multi-bit digital signal, and a second analog signal that is indicative of **said sum of values of said bits** in the multi-bit digital signal.

Consequently, the proposed combination does not teach or suggest a system comprising "means for receiving a multi-bit digital signal; means for generating at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that_is indicative of **said sum of values of said bits** in the multi-bit digital signal; and means for filtering at least two of the at least two analog signals,

including the first analog signal and the second analog signal", as recited in claim 17 (emphasis added).

Accordingly, claim 17, and claims 18-20 depending therefrom, should now be allowed.

Claims 29 and 30-38

Claim 29 recites a method comprising "receiving a multi-bit digital signal; generating at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of **said sum of values of said bits** in the multi-bit digital signal; and providing at least two of the at least two analog signals to a signal conditioning stage, the at least two of the at least two analog signals including the first analog signal and the second analog signal." (emphasis added).

Fling does not teach or suggest generating "a first analog signal that is indicative of a sum of values of bits" in a multi-bit digital signal, and "a second analog signal that is indicative of **said sum of values of said bits** in the multi-bit digital signal", as recited in claim 29 (emphasis added).

As stated above, Fling teaches that each of the DACs 16 and 18 receives its **own** data bits and outputs one analog signal indicative of a sum of values of those bits. Fling does not show two analog signals being indicative of the same sum of values of bits.

Consequently, the proposed combination does not teach or suggest a method comprising "receiving a multi-bit digital signal; generating at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of **said sum of values of said bits** in the multi-bit digital signal; and providing at least two of the at least two analog signals to a signal conditioning stage, the at least two of the at least two analog signals including the first analog signal and the second analog signal." (emphasis added).

Accordingly, claim 29, and claims 30-38 depending therefrom, should now be allowed.

Claims 39 and 40-48

Claim 39 recites a system comprising "means for generating at least two analog signals in response to a multi-bit digital signal, the at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital input signal and a

second analog signal that is indicative of **said sum of values of said bits** in the multi-bit digital signal; and a signal conditioning stage that receives at least two of the at least two analog signals, including the first analog signal and the second analog signal." (emphasis added).

As stated above with respect to claim 29, Fling does not teach or suggest generating a first analog signal that is indicative of a sum of values of bits in a multi-bit digital signal, and a second analog signal that is indicative of **said sum of values of said bits** in the multi-bit digital signal.

Consequently, the proposed combination does not teach or suggest a system comprising "means for generating at least two analog signals in response to a multi-bit digital signal, the at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital input signal and a second analog signal that is indicative of **said sum of values of said bits** in the multi-bit digital signal; and a signal conditioning stage that receives at least two of the at least two analog signals, including the first analog signal and the second analog signal", as recited in claim 39 (emphasis added).

Accordingly, claim 39, and claims 40-48 depending therefrom, should now be allowed.

<u>Claims 47-48</u>

Claims 47-48 are multiple dependent claims that each depend from claim 17 or 39 and are therefore also allowable.

<u>Rejections of Claims 5, 6-12 and 52 Under 35 U.S.C. §102</u>

Paragraph 5 of the Office Action rejects claims 5-12 under 35 U.S.C. §102 as being anticipated by Myers, 5,798,724.

The Office Action states that Myers discloses, in Fig. 1, a first conversion stage 22 receiving an N bit data signal at an input rate and a second conversion stage 26 in combination with interpolation stage 30 for providing an output analog signal 32 at an interpolation rate which is a multiple of the input rate.

Applicants traverse the rejection.

Claim 5 recites a system comprising "a DAC that receives a sequence of digital input signals at an input data rate and outputs a sequence of analog signals to a signal conditioning

stage at an output data rate, **each of the analog signals being indicative of an associated one of the digital input signals**, the magnitude of the output data rate being different than the magnitude of the input data rate, wherein more than one of the analog signals is generated during a single digital to analog conversion cycle of the DAC." (emphasis added).

Myers does not teach or suggest a DAC that receives a sequence of digital input signals at an input data rate and outputs a sequence of analog signals at an output data rate, wherein the magnitude of the output data rate is different than the magnitude of the input data rate and "**each of the analog signals being indicative of an associated one of the digital input signals**", as recited in claim 5 (emphasis added).

Myers discloses a digital-to-analog conversion method and interpolating digital-to-analog converter for a data modulation system which reduces the spurious energy content of the output signal (Abstract, lines 1-4). A first conversion stage converts the first n bits of an N bit data signal received at an input rate to a first output value (Abstract, lines 9-11). A second converter stage converts the remainder of the N bits and combines signals from the two conversion stages to provide a combined output (Abstract, lines 11-14). The combined output is provided to an interpolation stage which provides an interpolated output at an interpolation output rate which is a multiple of the input rate. (Abstract, lines 14-16).

Thus, Myers discloses a system that receives digital data at an input rate and provides interpolated analog output at an interpolation output rate, where the interpolation output rate is different than the input rate. However, Myers does not teach or suggest a sequence of analog signals at an output data rate different from the input data rate, with "**each of the analog signals being indicative of an associated one of the digital input signals**", as recited in claim 5 (emphasis added). For example, in the interpolated output of Myers, the signals that cause the interpolation rate to exceed the input rate are generated by interpolation, and therefore, are inherently not indicative of an **associated one** of the digital input signals.

Indeed, the Office Action is silent as to how Myers could possibly teach or suggest a sequence of analog signals at an output data rate different from the input data rate, wherein "**each of the analog signals being indicative of an associated one of the digital input signals**", as recited in claim 5 (emphasis added).

Consequently, Myers does not teach or suggest the system of claim 5.